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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,164	03/25/2004	Robert J. Schultz	RSTN-114	7766

30139 7590 02/22/2008

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EXAMINER	
CHOI, EUNSOOK	

ART UNIT	PAPER NUMBER
2619	

MAIL DATE	DELIVERY MODE
02/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/809,164	SCHULTZ, ROBERT J.	
	Examiner	Art Unit	
	Eunsook Choi	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The In the reply filed on 11/20/2007, the following has occurred:

- Claims 1, 6, and 18 are amended and claim 19 is canceled.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 12, is rejected under 35 U.S.C. 102(b) as being anticipated by Key et al. (US Patent 6272621).

Regarding claim 12, Key teaches in Fig. 3 a programmable arrayed processing engine, the first PE 400 – an array of processing element having at least one first stage processing element, the second row PE 400 – at least one second stage processing element, the first 330- a first stage memory unit that is searched in response to search information from the first stage processing element. Key teaches in Col. 13 Lines 45-55 a conventional encryption algorithm, such as data encryption standard (DES), may be modified to accommodate the multi-staged processing element pipeline where actual DES lookups are performed by the processing element stages using their partitioned memory resources 280 in accordance with the programmed instructions. That is, the entire packet is apportioned and fed through the stages of the pipeline where encryption

functions are performed (search-independent processing) in software (to perform search-independent processing related to a packet in parallel with a search of the first stage memory unit). Key teaches the encryption functions are performed in software in parallel with DES lookups. It is inherent in Key to allow the second stage processing element to perform search-independent processing.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 3, 5-7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Van Lunteren et al. (US Patent 7193997).

Regarding claim 1, Key teaches in Fig. 3 a programmable arrayed processing engine, the first 330 – performing a first search related to a packet using first search information. Key further teaches in Col. 13 Lines 45-55 an example of a conventional encryption algorithm, such as data encryption standard (DES), may be modified to accommodate the multi-staged processing element pipeline where actual DES lookups are performed by the processing element stages using their partitioned memory resources 280 in accordance with the programmed instructions. That is, the entire packet is apportioned and fed through the stages of the pipeline where encryption

functions are performed in software (performing, in parallel with the first search, search-independent processing on information related to the packet). Key teaches the encryption functions are performed in software in parallel with the search; however, Key does not expressly teach performing search-dependent processing using the result a result from the first search and a result of the search-independent processing to produce second search information. Van Lunteren teaches in Fig. 10 parallel lookups are combined to produce search information. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have performing search-dependent processing using the result a result from the first search and a result of the search-independent processing to produce second search information in order to allow highly efficient use of the TCAM (Col. 6 Lines 54-56, Van Lunteren).

Regarding claim 6, Key teaches in Fig. 3 a programmable arrayed processing engine, the first PE 400 - processing information using a first stage processing element to produce a first search key, wherein the first stage processing element is included within an array of processing elements, the first 330 – searching a first stage memory unit using the first search key. Key teaches in Col. 13 Lines 45-55 a conventional encryption algorithm, such as data encryption standard (DES), may be modified to accommodate the multi-staged processing element pipeline where actual DES lookups are performed by the processing element stages using their partitioned memory resources 280 in accordance with the programmed instructions. That is, the entire packet is apportioned and fed through the stages of the pipeline where encryption

functions are performed (search-independent processing) in software (performing, in parallel with the search of the first stage memory unit, search-independent processing on information related to the packet). Key teaches the encryption functions are performed in software in parallel with the search, however, Key does not expressly teach performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key, searching a second stage memory unit using the second search key. Van Lunteren teaches in Fig. 10 the resulting segment identifiers from the lookups are combined to produce a search key. This search key is supplied to a TCAM where it is compared with a set of ternary classification vectors. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have performing, at the second stage processing element, search-dependent processing using a result from the search of the first stage memory unit and a result of the search-independent processing to produce a second search key, searching a second stage memory unit using the second search key in order to allow highly efficient use of the TCAM (Col. 6 Lines 54-56, Van Lunteren).

Regarding claim 2, Key and Van Lunteren teach the limitations for claim 1 as applied above. Van Lunteren teaches in Fig. 10 performing a second search using the second search information.

Regarding claims 3 and 7, Key and Van Lunteren teach the limitations for claims 2 and 6 as applied above. Key teaches in Fig. 8 row synchronization logic (RSL) 800 ensuring that each PE stage completes its processing of current context prior to loading

new context at a new phase (holding a processing state from the search-independent processing until the result from the first search is available).

Regarding claim 11, Key and Van Lunteren teach the limitations for claim 6 as applied above. However, Key and Van Lunteren do not expressly teach forwarding information related to the packet to the second stage processing element before the result from the search of the first stage memory is produced. Key teaches in Fig. 8 row synchronization logic (RSL) 800 ensuring that each PE stage completes its processing of current context prior to loading new context at a new phase. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to forward information related to the packet to the second stage, the transient stage as shown in Fig. 8, processing element before the result from the search of the first stage memory is produced in order to allow additional processing of the transient data without stalling the remaining pipelines (Col. 4 Lines 51-52, Key).

6. Claims 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) in view of Kaganoi et al. (US PGPUB 20030012198).

Regarding claim 18, Key teaches in Fig. 3 a programmable arrayed processing engine, 400 - an array of processing elements, the first row of PEs - a plurality of first stage processing elements, the second row of PEs - a plurality of second stage processing elements, 310 - a memory interface that is configured to provide search information to a first stage memory unit from the plurality of first stage processing

elements. Key further teaches in Col. 13 and Lines 45-55 an example of a conventional encryption algorithm, such as data encryption standard (DES), may be modified to accommodate the multi-staged processing element pipeline where actual DES lookups are performed by the processing element stages using their partitioned memory resources 280 in accordance with the programmed instructions. That is, the entire packet is apportioned and fed through the stages of the pipeline where encryption functions are performed (search-independent processing) in software (the first and second stage processing elements are configured to allow the second stage processing elements to perform search-independent processing related to respective packets in parallel with searches of the first stage memory unit). However, Key does not expressly teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directrly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste of all times (Paragraph 50, Kaganoi).

Regarding claim 20, Key and Kaganoi teach the limitations for claim 18 as applied above. However, Key and Kaganoi do not expressly teach forward information to respective second stage processing elements before results from respective searches of the first stage memory unit are received by the second stage processing elements. Key teaches in Fig. 8 row synchronization logic (RSL) 800 ensuring that each

PE stage completes its processing of current context prior to loading new context at a new phase. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to forward information related to the packet to the second stage, the transient stage as shown in Fig. 8, processing element before the result from the search of the first stage memory is produced in order to allow additional processing of the transient data without stalling the remaining pipelines (Col. 4 Lines 51-52, Key).

Regarding claim 21, Key and Kaganoi teach the limitations for claim 18 as applied above. Key teaches in Fig. 3 330 - memory bus.

7. Claims 4, 5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) modified by Van Lunteren et al. (US Patent 7193997) as applied to claims 1 and 6 above, and further in view of Khanna (US Patent 7219187).

Regarding claims 4 and 10, Key and Van Lunteren teach the limitations for claims 2 and 6 as applied above. However, Key and Van Lunteren do not teach producing a comparand and a mask as the second search information. Khanna teaches in Col. 2 Lines 10-19 the CAM device can be instructed by the processor to compare a search key, also referred to as a comparand (e.g., generated from packet header data), with data stored in its associative memory array. Khanna further teaches in Col. 9 Lines 31-62 global mask select circuit 607 selects the corresponding global mask ID (GMID 622) from search parameter table 525 in response to the activated GMSEL signal. The selected GMID is used to select a corresponding global mask

GM(1) GM(z) from the global mask register 606 that globally masks the comparand data during a compare operation. It would be obvious to one having ordinary skill in the art at the time of the invention was made to produce a comparand and a mask as the second search information in order for routers and CAM devices to perform the various lookups on packets (Col. 2 Lines 10-19 Khanna).

Regarding claim 5, Key, Van Lunteren, and Khanna teach the llimitations for claim 4. Khanna teaches in Fig. 6 and Col. 9 Lines 31-62 Block select circuit 605 outputs block select signal BSEL 609 that enables comparand drivers 608 to drive the comparand data into CAM block array 602 to participate in a compare operation if a stored CAM table ID for the CAM array 602 matches one of the CAM table IDs provided from the search parameter table 525. the comparand data is globally masked by the selected global mask data by logically ANDing together the selected global mask data on a bit-for-bit basis with corresponding bits of the comparand data in the comparand drivers 608.

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) modified by Van Lunteren et al. (US Patent 7193997) as applied to claims 6 and 7 above, and further in view of Kaganoi et al. (US PGPUB 20030012198).

Regarding claims 8 and 9, Key and Van Lunteren teach the limitations for claims 6 an 7 as applied above. However, Key and Van Lunteren do not expressly teach to provide search results from the first stage memory unit directly to the plurality of second

stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directrly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste of all times (Paragraph 50, Kaganoi).

9. Claims 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) as applied to claim 12, and in view of Kaganoi et al. (US PGPUB 20030012198).

Regarding claims 13, Key teaches the limitations for claim 12 as applied above. However, Key does not expressly teach to provide search results from the first stage memory unit directly to the plurality of second stage processing elements. Kaganoi teaches in Fig.3 search results from CAM 13 and Associated Data Memory 15 are directrly provided to the next processing stages. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide search results from the first stage memory unit directly to the plurality of second stage processing elements in order to perform the retrieval processing without waste of all times (Paragraph 50, Kaganoi).

Regarding claim 17, Key teaches the limitations for claim 12. Kaganoi teaches in Fig.3 first stage memory unit comprises content addressable memory.

10. Claims 14, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Key et al. (US Patent 6272621) as applied to claim 12 above, and in view of Van Lunteren et al. (US Patent 7193997).

Regarding claim 14, Key teaches the limitations for claim 12 as applied above. However, Key does not expressly teach the second stage processing element is further configured to perform search-dependent processing using a result of the search of the first stage memory unit and a result from the search-independent processing to produce a search key. Van Lunteren teaches in Fig. 10 parallel lookups are combined to produce a search key. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a single search key lookup operation is treated as a multidimensional packet classification problem allowing highly efficient use of the TCAM (Col. 6 Lines 54-56, Van Lunteren).

Regarding claim 15, Key and Van Lunteren teach the limitations for claim 14. Van Lunteren teaches in Fig. 10 a second stage memory unit that is associated with the second stage processing element, wherein the search key is used to search the second stage memory unit.

Regarding claim 16, Key and Van Lunteren teach the limitations for claim 15. Key teaches in Fig. 3 and Col. 13 and Lines 45-55 an example of a conventional encryption algorithm, such as data encryption standard (DES), may be modified to accommodate the multi-staged processing element pipeline where actual DES lookups are performed by the processing element stages using their partitioned memory resources 280 in accordance with the programmed instructions. That is, the entire packet is apportioned

and fed through the stages of the pipeline where encryption functions are performed (search-independent processing) in software. It is inherent in Key and Van Lunteren the second and third stage processing elements are configured to allow the third stage processing element to perform search-independent processing related to the packet in parallel with the search of the second stage memory unit.

Response to Arguments

11. Applicant's arguments, filed 11/20/2007, with respect to the rejection(s) of claim(s) 1-21 under 35 U.S.C. 102(e) and 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Key et al. (US Patent 6272621).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eunsook Choi whose telephone number is 571-270-1822. The examiner can normally be reached on Monday-Friday 8:00-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
2/11/2008

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